

Amended Claims

1. (withdrawn) A LVTSCR-like structure having one or more diodes formed in a p-well of the structure.
2. (currently amended) A method of increasing the holding voltage of an LVTSCR structure that includes an n-well and a p-well formed in a substrate, a gate, a first n+ region and a first p+ region formed in the n-well to define a high voltage node on one side of the gate, and a second n+ region and a second p+ region formed in the p-well to define a low voltage node on the other side of the gate, the method comprising forming ~~an at least one additional p+ region and at least one additional n+ region inside the p-well of the structure to define a at least one p-n junction between a the p-type material as defined by the p-well and the second p+ region one of the additional p+ regions in the p-well on the one hand, and an the n-type material as defined by the additional n+ region of one of the additional n+ regions in the p-well on the other hand,~~ the p-n junction being forward biased during normal operation by having said additional n+ region ~~p+ region~~ of the p-n junction located further from ~~closer to~~ the high voltage node than the second p+ region ~~additional n+ region of the p-n junction.~~
3. (previously presented) A method of increasing the holding voltage of an LVTSCR structure having an anode in an n-well and a cathode in a p-well, the cathode being defined by an n+ region and a p+ region, comprising
forming at least one additional n+ region and at least one additional p+ region in the p-well to define at least one forward biased diode under normal operation in the p-well, thereby providing an alternative current path from anode to cathode through said at least one diode.
4. (original) A method of claim 3, wherein the alternative current path defines a lower resistance current path than the p-well.
5. (canceled)
6. (canceled)

7. (canceled)
8. (canceled)
9. (new) A method of claim 2, further comprising forming at least one additional p⁺ region and multiple additional n⁺ regions inside the p-well of the structure to define multiple p-n junctions in the p-well, each p-n junction being formed between a p-type material as defined by the p-well and one of the additional p⁺ regions or the second p⁺ region, and n-type material as defined by one of the additional n⁺ regions.